ATME COLLEGE OF ENGINEERING

13th KM Stone, Bannur Road, Mysore - 570 028

DEPARTMENT OF ELECTRICAL & ELECTRONICS ENGINEERING

NOTES

Course Title : Digital Logic Circuits

Course CODE: BEE306A

SEMESTER: III

Academic Year - 2025-26

INSTITUTIONAL VISION AND MISSION

VISION:

- Development of academically excellent, culturally vibrant, socially responsible and globally competent human resources.

MISSION:

- To keep pace with advancements in knowledge and make the students competitive and capable at the global level.
- To create an environment for the students to acquire the right physical, intellectual, emotional and moral foundations and shine as torchbearers of tomorrow's society.
- To strive to attain ever-higher benchmarks of educational excellence.

Department Vision and Mission

Vision:

To create Electrical & Electronics Engineers who excel to be technically competent and fulfill the cultural and social aspirations of the society.

Mission:

- To provide knowledge to students that builds a strong foundation in the basic principles of electrical engineering, problem solving abilities, analytical skills, soft skills and communication skills for their overall development.
- To offer outcome based technical education.
- To encourage faculty in training & development and to offer consultancy through research & industry interaction.

Program Educational Objectives (PEOs)

PEO1:

To produce competent and ethical Electrical and Electronics Engineers who will exhibit the necessary technical and managerial skills to perform their duties in society.

PEO2:

To make Graduates continuously acquire and enhance their technical and socio-economic skills.

PEO3:

To aspire Graduates on R & D activities leading to offering solutions and excel in various career paths.

PEO4:

To produce quality engineers who have the capability to work in teams and contribute to real time projects

Program Outcomes (POs)

Engineering Graduates will be able to:

PO1: Engineering Knowledge: Apply the knowledge of mathematics, science, engineering fundamentals and an engineering specialization to the solution of complex engineering problems.

PO2: Problem Analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3: Design / Development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4: Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5: Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO6: The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7: Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8: Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9: Individual and team work: Function effectively as an individual and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10: Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11: Project management and finance: Demonstrate knowledge and understanding of the engineering management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12: Life-long learning: Recognize the need for and have the preparation and ability to engage in independent and lifelong learning in the broadest context of technological change.

Program Specific Outcomes (PSOs)

The students will develop an ability to produce the following engineering traits:

PSO1:Apply the concepts of Electrical & Electronics Engineering to evaluate the performance of power systems and also to control industrial drives using power electronics

PSO2: Demonstrate the concepts of process control for Industrial Automation, design models for environmental and social concerns and also exhibit continuous self- learning

Digital Logic Circuit

				Academic Year: 2025-2026			
Department: Electrical and Electronics Engineering							
Course Code	Course Title	Core/Elective	Prerequisite	Contact Hours			Total Hrs/ Sessions
				L	T	P	
BEE306A	**Digital Logic Circuit**	**Elective**	**Basic Electronics**	**3**	**-**	-	**40 theory**

Topics Covered as per Syllabus

Module-1

Definition of combinational logic, canonical forms, Generation of switching equations from truth tables, Karnaugh maps-3,4,5 variables, Incompletely specified functions (Don‘t care terms) Simplifying Max term equations, Quine-McCluskey minimization technique, Quine-McCluskey using don‘t care terms, Reduced prime implicants Tables.

Module-2

General approach to combinational logic design, Decoders, BCD decoders, Encoders, digital multiplexers, Using multiplexers as Boolean function generators, Adders and subtractors, Cascading full adders, Look ahead carry, Binary comparators

Module-3

Basic Bistable elements, Latches, Timing considerations, The master-slave flip-flops (pulsetriggered flip-flops): SR flip-flops, JK flip-flops, Edge triggered flip- flops, Characteristic equations

Module-4

Registers, binary ripple counters, synchronous binary counters, Counters based on shift registers, Design of a synchronous counter, Design of a synchronous mod-n counter using clocked T, JK, D and SR flip-flops.

Module-5

Mealy and Moore models, State machine notation, Synchronous Sequential circuit analysis, Construction of state diagrams, counter design.

Memories: Read only and Read/Write Memories, Programmable ROM, EPROM, Flash memor**y.**

List of Text Books

“Digital Logic Applications and Design” by John M Yarbrough, 2011 edition.
“HDL Programming (VHDL and Verilog)” by Nazeih M. Botros, 1 st Edition
“Digital Principles and Design “, Donald D Givone, Tata McGraw Hill Edition,2002.

List of Reference Books

“Logic Design” by RD Sudhaker Samuel

List of URLs, Text Books, Notes, Multimedia Content, etc: https://www.youtube.com/watch?v=VnZLRrJYa2I

MODULE 3

Flip Flops and Characteristic Equation

Structure

- Objective
- Introduction
- Basic Bistable element
- Latches, SR latch,
- Application of SR latch,-A Switch debouncer.
- The gated SR latch.
- The gated D Latch
- The Master-Slave Flip-Flops (Pulse-Triggered Flip-Flops): The master-slave SR Flip-Flops, Themaster-slave JK Flip-Flop,
- Edge Triggered Flip-flop: The Positive Edge-Triggered D Flip-Flop, Negative-Edge TriggeredD Flip-Flop - Characteristic equations.

Objevtive

- To know different between latches and flip flops
- Data storage elements
- Designing of flip flops

Introduction

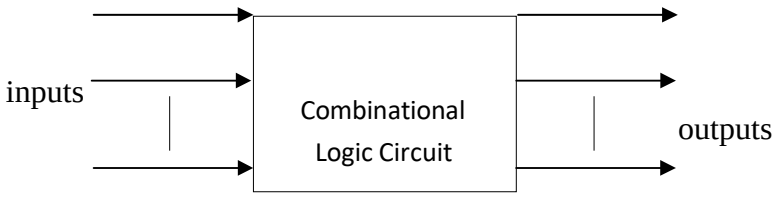
Logic circuit is divided into two types.

1. Combinational Logic Circuit
2. Sequential Logic Circuit

Definition:

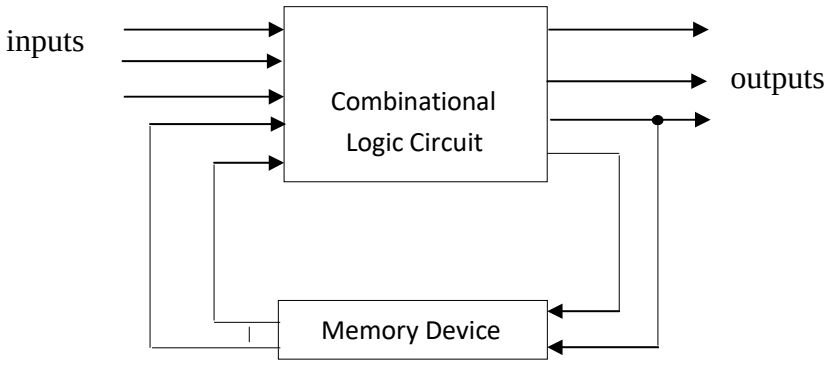
1. Combinational Logic Circuit :

   The circuit in which outputs depends on only present value of inputs. So it is possible to describe each output as function of inputs by using Boolean expression. No memory element involved. No clock input. Circuit is implemented by using logic gates. The propagation delay depends on, delay of logic gates. Examples of combinational logic circuits are: full adder, subtractor, decoder, code converter, multiplexers etc.



2. Sequential Circuits :

Sequential Circuit is the logic circuit in which output depends on present value of inputsat that instant and past history of circuit i.e. previous output. The past output is stored by using memory device. The internal data stored in circuit is called as state. The clock is required for synchronization. The delay depends on propagation delay of circuit and clock frequency. The examples are flip-flops, registers, counters etc.



Basic Bistable element

- Flip-Flop is Bistable element.
- It consist of two cross coupled NOT Gates.
- It has two stable states.
- Q and □Q are two outputs complement of each other.
- The data stored 1 or 0 in basic bistable element is state of flip-flop.
- 1 – State is set condition for flip-flop.
- 0 – State is reset / clear for flip-flop.
- It stores 1 or 0 state as long power is ON.

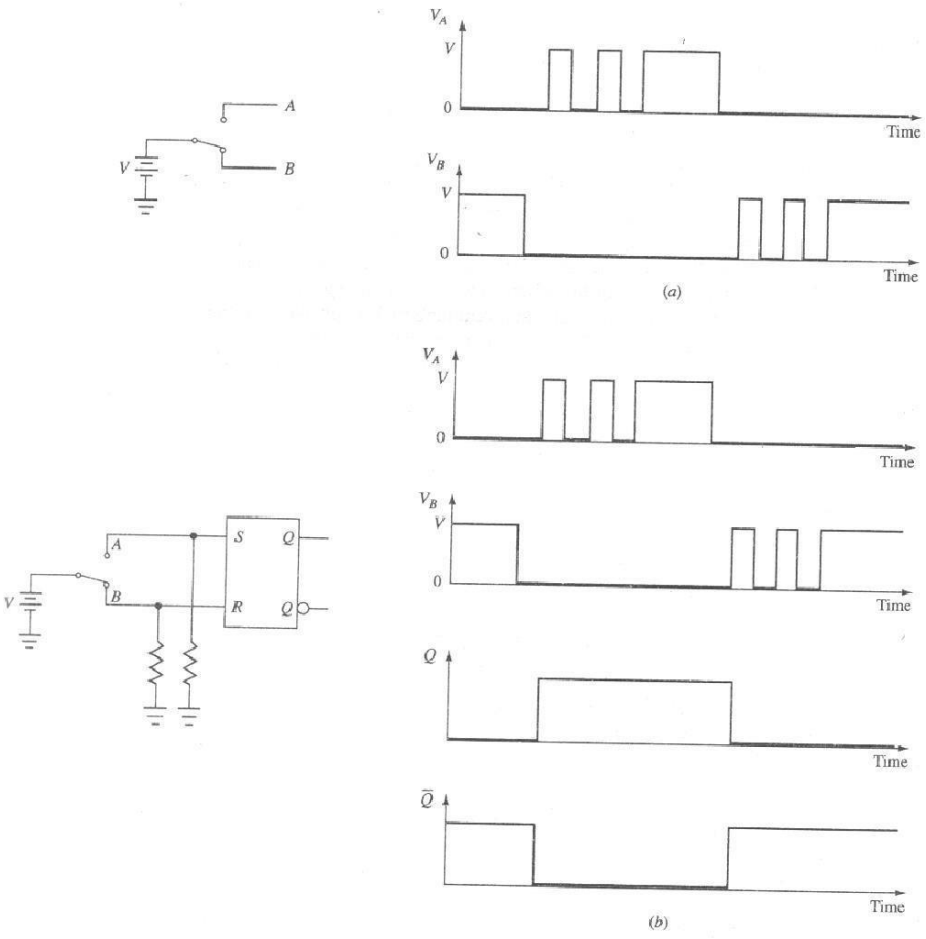
Latches, SR latch

S-R Latch : Set-reset Flip-Flop

- Latch is a storage device by using Flip-Flop.
- Latch can be controlled by direct inputs.
- Latch outputs can be controlled by clock or enable input.
- Q and □Q are present state for output.
- Q^+ and □Q^+ are next states for output.
- The function table / Truth table gives relation between inputs and outputs.
- The S=R=1 condition is not allowed in SR FF as output is unpredictable.

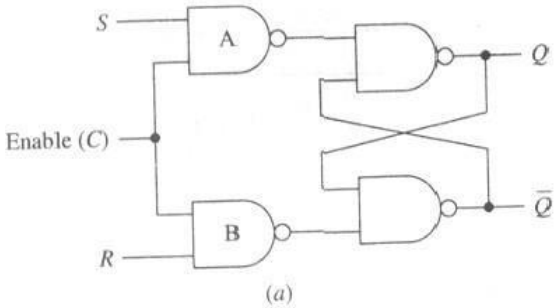
Application of SR latch- A Switch debouncer.

- A switch debouncer



- Bouncing problem with Push button switch.
- Debouncing action.
- SR Flip-Flop as switch debouncer.

The gated SR latch. Characteristic equations,

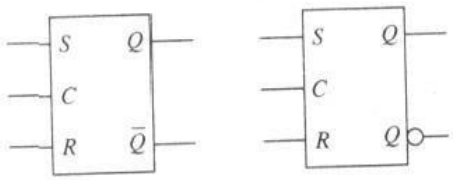


(a)

Inputs			Outputs	
S	R	C	Q^+	$\bar{Q}^+$
0	0	1	Q	$\bar{Q}$
0	1	1	0	1
1	0	1	1	0
1	1	1	1*	1*
X	X	0	Q	$\bar{Q}$

*Unpredictable behavior will result if S and R return to 0 simultaneously or C returns to 0 while S and R are 1

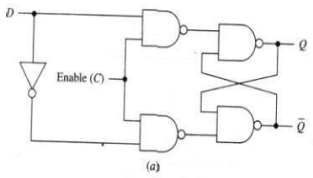
(b)



(c)

- Enable input C is clock input.
- C=1, Output changes as per input condition.
- C=0, No change of state.
- S=1, R=0 is set condition for Flip-flop.
- S=0, R=1 is reset condition for Flip-flop.
- S=R=1 is ambiguous state, not allowed.

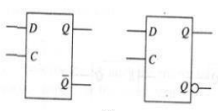
The gated D Latch Characteristic equations,



(a)

Inputs		Outputs	
D	C	Q^+	$\bar{Q}^+$
0	1	0	1
1	1	1	0
X	0	Q	$\bar{Q}$

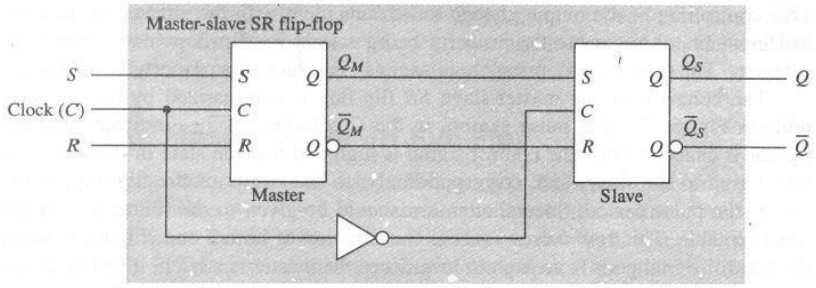
(b)



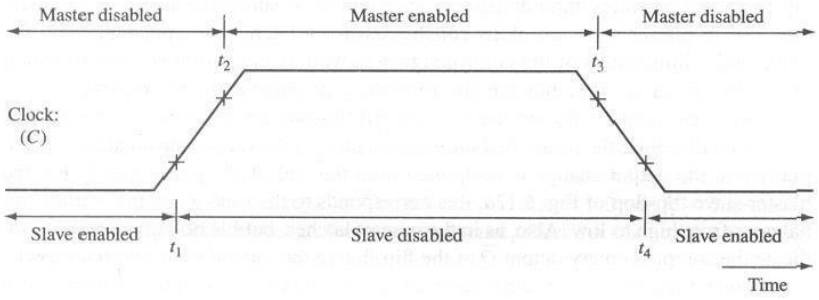
(c)

- D Flip-Flop is Data Flip-Flop.
- D Flip-Flop stores 1 or 0.
- R input is complement of S.
- Only one D input is present.
- D Flip-Flop is a storage device used in register.

The Master-Slave Flip-Flops (Pulse-Triggered Flip-Flops): The master-slave SR Flip-Flops, The master-slave JK Flip-Flop Characteristic equations,



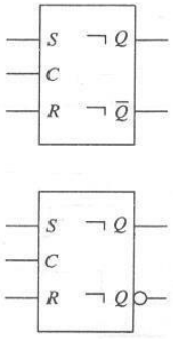
(a)



(b)

Inputs			Outputs	
S	R	C	Q^+	$\overline{Q}^+$
0	0		Q	$\overline{Q}$
0	1		0	1
1	0		1	0
1	1		Undefined	Undefined
X	X	0	Q	$\overline{Q}$

(c)

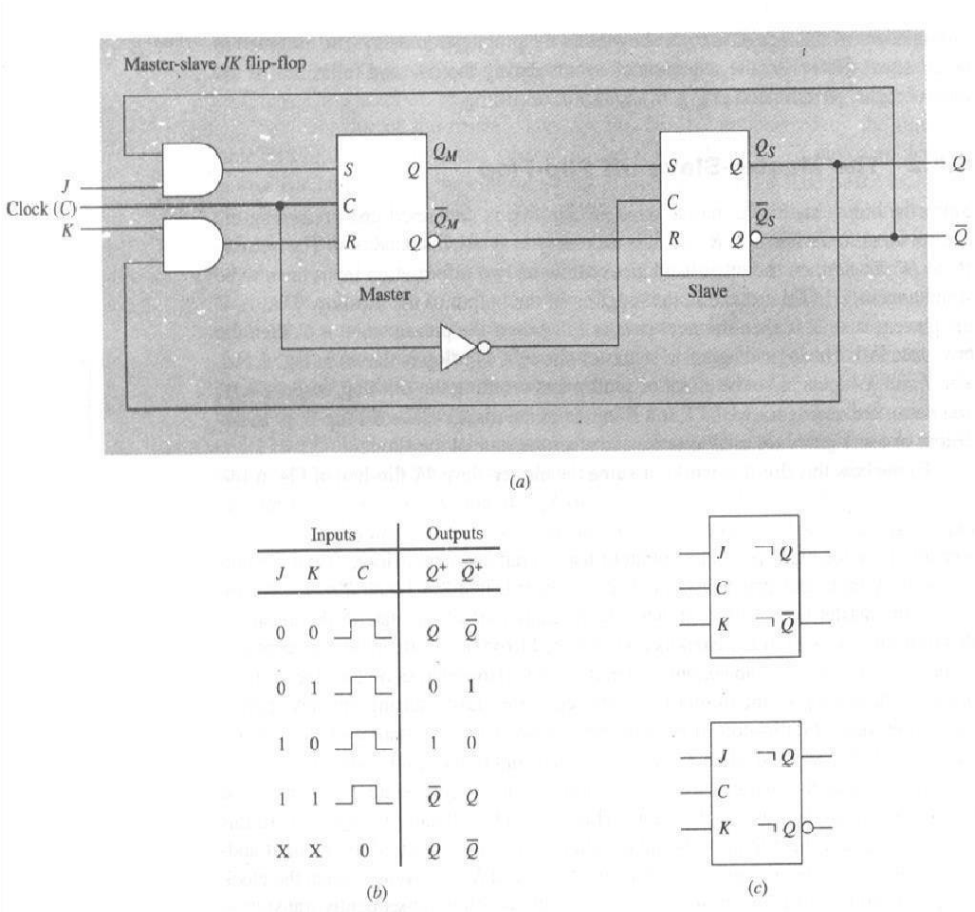


(d)

- Two SR Flip-Flop, 1st is Master and 2nd is slave.
- Master Flip-Flop is positive edge triggered.
- Slave Flip-Flop is negative edge triggered.

- Slave follows master output.
- The output is delayed.

Master slave JK Flip-Flop Characteristic equations,

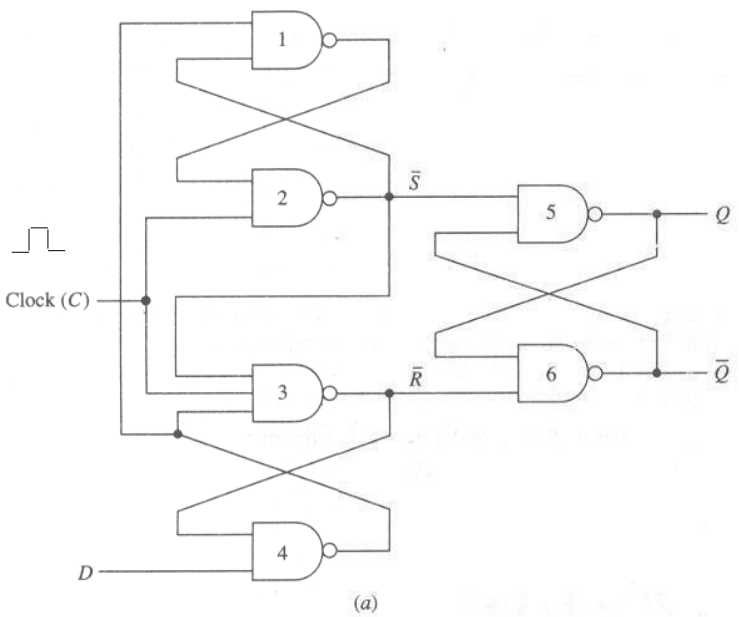


- In SR Flip-Flop the input combination S=R=1 is not allowed.
- JK FF is modified version of SR FF.
- Due to feedback from slave FF output to master, J=K=1 is allowed
- J=K=1, toggle, action in FF.

This finds application in
counter.

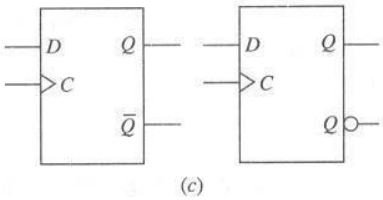
Edge Triggered Flip-flop: The Positive Edge-Triggered D Flip-Flop, Negative-EdgeTriggered D Flip-Flop. Characteristic equations,

Positive Edge Triggered D Flip-Flop



Inputs		Outputs	
D	C	Q^+	$\bar{Q}^+$
0	↑	0	1
1	↑	1	0
X	0	Q	$\bar{Q}$
X	1	Q	$\bar{Q}$

(b)



- When C=0, the output of AND Gate 2 & 3 is equal to 1.
  S̶ □ R̶ □ 1, No Change of State
- If C=1, D=1, the output of AND Gate 2 is 0 and 3 is 1.
  $\bar{S}$ □ 0, $\bar{R}$ □ 1, Q =1 and Q $\bar{\square}$ 0